A640H

Uncooled Thermal Imaging Module

Product Manual

V1.0.0

Historical Versions

Version	Date	Description
V1.0.0	2024-08	Initial release

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1 Product Description

The A640H series uncooled infrared module offers a variety of lenses and multiple user expansion components to choose from. Designed for high-reliability applications, it provides a trusted solution widely used in outdoor observation, integrated gimbals, and driver assistance systems.

2 Lens Type

Table 2.1 Lens Parameters

Array Size	Focal Length/F#	Lens type	HFOV×VFOV	IFOV
640×512	4.1mmF1.2	Athermalized	89°×75°	2.92mrad
	6.9mmF1.0	Athermalized	63°×50°	1.74mrad
	9.1mmF1.2	Athermalized	48°×38°	1.31mrad
	13mmF1.2	Athermalized	33°×26°	0.92mrad
	19mmF1.0	Athermalized	22°×18°	0.63mrad
	25mmF1.0	Athermalized	17°×14°	0.48mrad
	35mmF1.0	Athermalized	12.5°×10°	0.34mrad
	55mmF1.0	Athermalized	8°×6.4°	0.21mrad
	75mmF1.0	Athermalized	5.9°×4.7°	0.16mrad
	100mmF1.0	Athermalized	4.4°×3.5°	0.12mrad

3 Product Performance Parameters

Table 3.1 Specifications (1)

Performance Indicators			
Detector Type		Uncooled VOx infrared detector	
Resolution		640×512	
Pixel pitch		12μm	
Detector Frame Rate		50Hz(60Hz optional)	
Spectral Band		8~14μm	
Noise Equivalent Temperature Difference (NETD)		＜40mK @25℃, F#1.0	
Time to Image		≤4s	
TEC		No	
Image Adjustment			
Brightness&Contrast Adjustment		Manual/Auto/Linear	
Polarity		Black-hot/White-hot	
Edge highlight		Supported	
Palette		Supported	
Reticle		Display/Blank/Move	
Digital Zoom		1.0~8.0× continuous zoom (step size: 0.1)	
Image Processing		Non-uniformity correction	
		Shutterless	
		Digital filtering noise reduction	
		Digital detail enhancement	
Mirroring		Horizontal/Vertical/Diagonal	
Power Supply			
Power Supply Range		3.9~5VDC	
		5~18V DC supported by user extension components	
Typical Service Voltage		4V DC	
Typical Power Consumption @25°C	Without user extension component	≤600mW	≤700mW
	With user extension component	≤800mW	≤850mW
Power Protection		Overvoltage, undervoltage, and reverse connection supported by user extension components	
Interface			
Video Output	Analog video	1-channel PAL system (2)	
	Digital video	BT656 interlaced mode	
		BT656 progressive mode	

		USB2.0
		DVP
Serial Communication Interface		USB2.0/RS232/UART (3.3V)
Physical Characteristics		
Weight (Without lens and extension components)		21g±1g
Dimensions (Without lens)		26mm×26mm
Environment Adaptability		
Operating Temperature		-40℃～+80℃
Storage Temperature		-45℃～+85℃
Humidity		5% to 95%, non-condensing
Vibration		6.06g, random vibration (3)
Shock		1000g@0.3ms(4)

Notes:

(1) Ambient test environment: temperature: 23 to 25℃, humidity: 50 to 55%RH, and standard atmospheric pressure: 101.325kPa, without lens.

(2) The analog video output uses the PAL-D system.

(3) This magnitude is for a single module.

(4) Single-module shock (without lens).

4 Description of User Interface of Module

The user interface of the module component adopts the design of HRS (Hirose) 70-Pin DF40C-70DP-0.4V (51) connectors, which contain interfaces for power supply, UART communication, analog video, 16-bit parallel data transmission, LVDS serial data transmission, and general-purpose input/output (GPIO). Users can connect to the module component using HRS DF40C-70DS-0.4V(51) connectors.

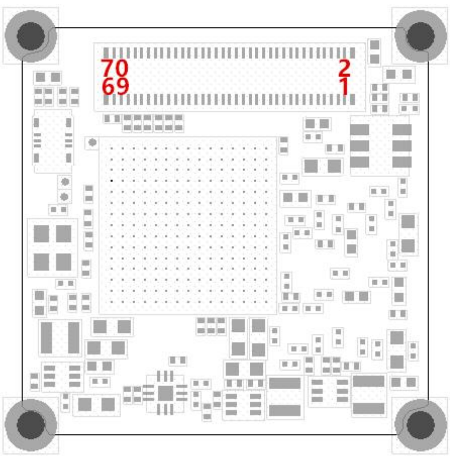


Figure 4.1 Module Component 70-Pin User Interface

4.1 Pinout of Hirose 70-Pin Connector User Interface

Table 4.1 User Interface Definition of HRS (Hirose) 70-pin Connector

Pin No.	Pin Name	Type	Description	
1, 2, 3, 4	MAIN_POWER	Power supply	Power input (3.9~5V DC) (1)	
5, 6, 7, 8, 13, 14, 17, 18, 43, 44, 55, 56, 69, 70	GND	Power supply	Power GND (3)	
9, 11	VIDEO1	Output	Analog Video	
10, 12	VGND	Power supply	Analog video GND	
15	RS232_TX	Output	RS232 communication (2)	
16	RS232_RX	Input		
46	UART_TX	Output	UART communication interface (3.3V) (2)	
45	UART_RX	Input		
57	GPIO0	Input/Output	General programmable input and output interface (1.8V)	
59	GPIO1	Input/Output		
61	GPIO2	Input/Output		
63	GPIO3	Input/Output		
65	GPIO4	Input/Output		
67	GPIO5	Input/Output		
47	GPIO6	Input/Output		
49	GPIO7	Input/Output		
51	GPIO8	Input/Output		
53	GPIO9	Input/Output		
25	DV0	Output	10/16-bit parallel digital video signal (3.3V)	Data signal LSB
26	DV1	Output		Data signal
27	DV2	Output		Data signal
28	DV3	Output		Data signal
29	DV4	Output		Data signal
30	DV5	Output		Data signal
31	DV6	Output		Data signal
32	DV7	Output		Data signal
33	DV8	Output		Data signal
34	DV9	Output		Data signal MSB (10-bit)
35	DV10	Output		Data signal
36	DV11	Output		Data signal
37	DV12	Output		Data signal
38	DV13	Output		Data signal

23	IO0/DV14	Input/Output		Data signal
24	IO1/DV15	Input/Output		Data signal MSB (16-bit)
39	FRAME_VALID	Output		Frame valid signal
40	LINE_VALID	Output		Row valid signal
42	CLKOUT	Output		Clock Signal
41	EXT_SYNC	Input/Output		External synchronization signal
48, 50, 52, 54, 58, 60, 62, 64, 66, 68	NC		Reserved	
19	TCK	Input/Output	JTAG (3.3V)	
20	TDI			
21	TMS			
22	TDO			

Notes:

(1) The typical power supply input voltage is 4V DC. All voltage here refers to the voltage to the module connector. Power input requirements: rise time (10%~90%) < 4ms; peak current > 1.0A.

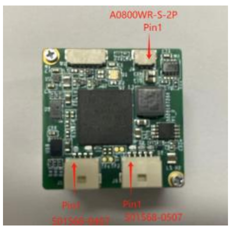
(2) Both TX and RX in the serial communication interface refer to the transmit and receive of the module;

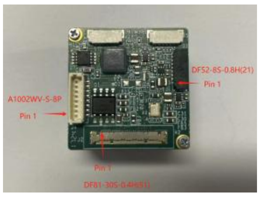
(3) GND and VGND are short-circuited inside the module.

(4) Common ground for the power ground and signal ground.

4.2 List of User Extension Component

Table 4.2 List of User Extension Component

Model	Figure	Main Interfaces/Functions
TAH02V110F016C		Power Supply: Powered by USB, typical voltage 5 VDC Communication: USB USB UVC digital video Analog video
TAH02V100F022C		Power Supply: Powered by USB, typical voltage 5 VDC Communication: USB RS422 USB UVC digital video Analog video

TAX000V100F012C		Power Supply: 4.5 to 18 VDC, typical voltage 12 VDC Communication: RS-232, UART Analog video BT.656 digital video
TAH02V100F031C		Power Supply: 6 to 18 VDC, typical voltage 12 VDC Communication: RS232 Analog video DVP digital video
TAH02V100F017C		Power Supply: 5 to 18 VDC, typical voltage 12 VDC Communication: UART, RS232, RS422 MIPI digital video Analog video

4.3 LVMOS

LVCMOS is a common digital video interface that allows parallel output. The DVP interface contains 1 clock signal line, 1 frame synchronization (field synchronization) signal line, 1 line synchronization signal line, 1 enable signal line, and 14 parallel data signal lines. When a data frame arrives, the frame synchronization signal goes high, indicating that the next data is the same data frame. When the frame is finished, the frame synchronization signal goes low, indicating the end of the data frame. Similarly, when a line of data arrives, the line synchronization signal goes high, and when the line of data is finished, the line synchronization signal goes low.

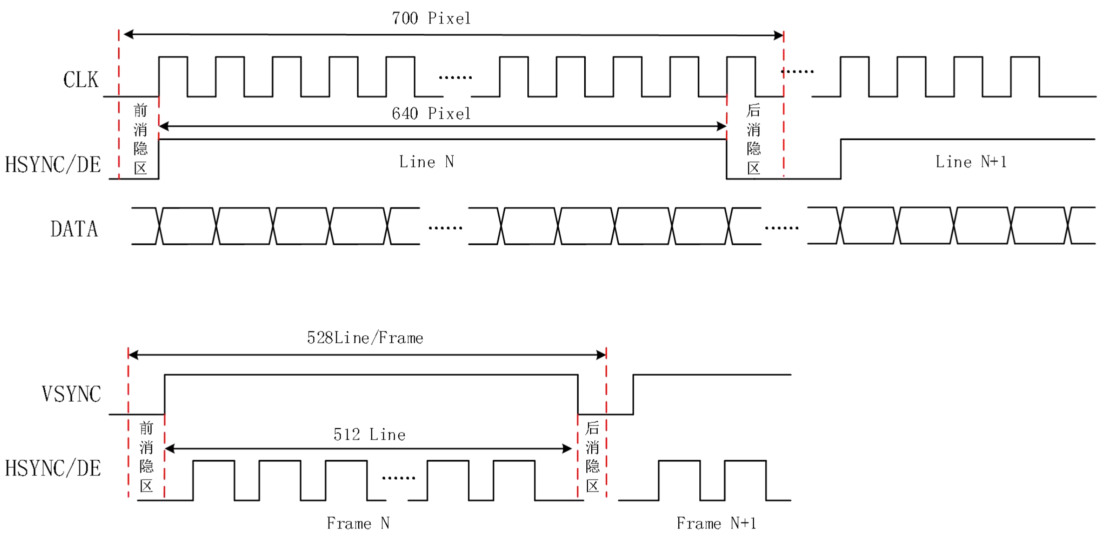


Figure 4.2 LVCMOS Timing Diagram

Table 4.3 LVCMOS Timing Description

No.	Signal	Description	Remarks
1	CLK	Clock	18.75MHz (=700×528×50Hz)
2	DATA	Data	Valid data: 640 pixels×512 lines
3	HSYNC	Line synchronization	There are 700 pixels in one line, of which 640 are valid data, and the remaining 60 are blanking data, with 30 pixels in the pre-blanking area and 30 pixels in the post-blanking area.
4	VSYNC	Frame synchronization	There are 528 lines in one frame, 512 of which are valid data lines, and the remaining 16 are blanking data lines.

4.4 BT656 Interlaced Mode

BT656 videos do not require a frame synchronization signal or a line synchronization signal but only one clock signal and eight cables.

In BT656 interlaced mode, the output array size of the module is 720×576, and the frame rate is 25Hz.

In interlaced mode, data in odd-numbered lines (1, 3, 5...) is output as the data of the odd field, and data in even-numbered lines (2, 4, 6...) is output as the data of the even field. The data of a frame is not arranged in sequence according to the line number, as shown in the table and figure below.

Table 4.4 BT656 Clock Frequency

Product Category	Clock Frequency
BT656 Interlaced	27MHz

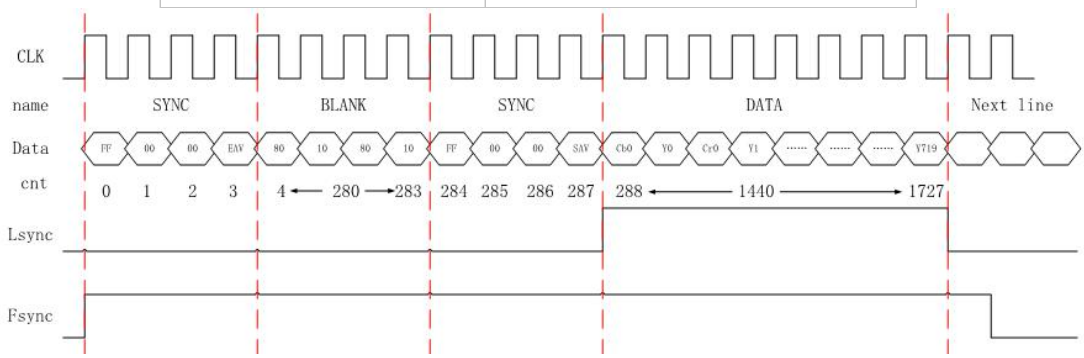


Figure 4.3 BT656 Interlaced Mode Timing

For BT656 videos, each line of data includes three parts: reference code (EAV/SAV), blanking area (Blanking), and data area (Active Video). Lines with effective data are called active lines, while those with ineffective data are called blanking lines. BT656 videos have no line or field synchronization signal. Therefore, flag bits of line or frame should be added to the 8-bit data to indicate the start and end of the line or frame. These flag bits are called synchronization reference codes. Each line contains 1,728 bytes of data consisting of a horizontal control signal and a YCbCr video data signal arranged in the order Cb-Y-Cr-Y. The first 288 bytes of the line represent the line control signal. Among these bytes, the first four bytes indicate the valid video end signal (EAV), which is followed by 140 "80, 10" fixed data blocks (totaling 280 bytes). The 288 bytes end with a 4-byte video start signal (SAV). The effective video data is next to the horizontal control signal and has 1440 bytes in total. Both the even field and odd field contain 288 lines and 720 pixels, and the entire field of the BT656 image has 576 lines and 720 pixels.

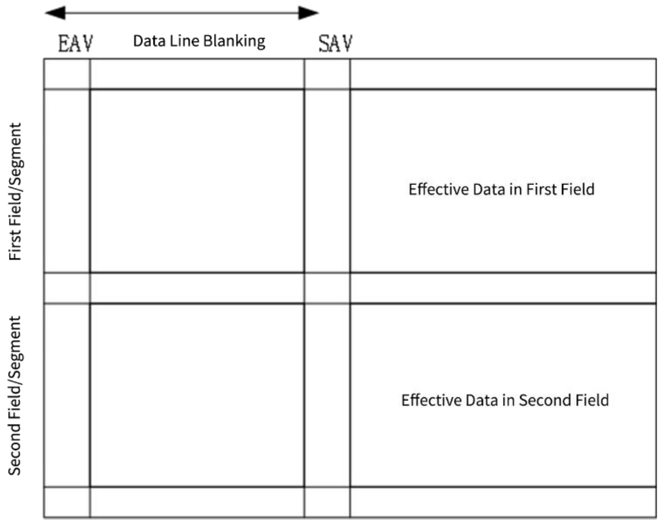


Figure 4.4 Fields/Segments Timing in Interlaced and Segmented Modes

See Figure 4.5 for specific output data:

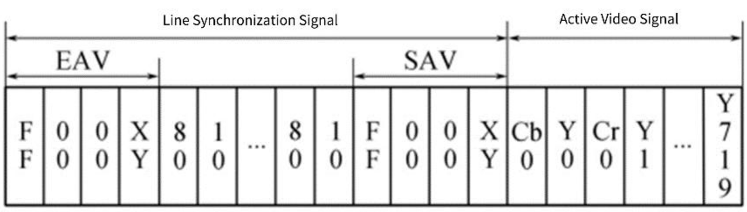


Figure 4.5 Output Data of Active Line

"FF, 00, 00" occupy the leading three bytes of SAV and EAV. "XY" in the last byte indicates the position of the line in the entire data frame and distinguishes between SAV and EAV. Refer to Table 6 for detailed information on "XY". F=0: Even field; F=1: Odd field; V=0: The line contains effective video data; V=1: The line contains no effective video data; H=0: SAV signal; H=1: EAV signal. P3~P0 are protection signals, which are generated based on F, V, and H following XOR rules. Specifically, P3=V xor H, P2=F xor H, P1=F xor V, and P0=F xor V xor H, based on which synchronization header detection is implemented. Detailed information is shown below:

Table 4.5 BT656 Synchronization Header Definition

bit	7	6	5	4	3	2	1	0
value	1	F	V	H	V xor H	F xor H	F xor V	F xor V xor H

Table 4.6 BT656 Data Distribution per Frame in Interlaced Mode

	0	1	2	3	4-283	284	285	286	287	288-1727
Line	EAV				Invalid	SAV				Valid
0-21	FF	00	00	B6	Y: 10 Cb/Cr: 80	FF	00	00	AB	Y: 10 Cb/Cr: 80
22-309	FF	00	00	9D		FF	00	00	80	YCbCr
310-311	FF	00	00	B6		FF	00	00	AB	Y: 10 Cb/Cr: 80
312-334	FF	00	00	F1		FF	00	00	EC	Y: 10 Cb/Cr: 80
335-622	FF	00	00	DA		FF	00	00	C7	YCbCr
623-624	FF	00	00	F1		FF	00	00	EC	Y: 10 Cb/Cr: 80

The output effective data is displayed in a 640×512 area array in the center, with the rest of the data filling in the black border.

4.5 BT656 Progressive Mode

BT656 progressive output indicates that data is output line by line.

Table 4.7 BT656 Clock Frequency

Product Category	Clock Frequency
BT656 Progressive	54MHz

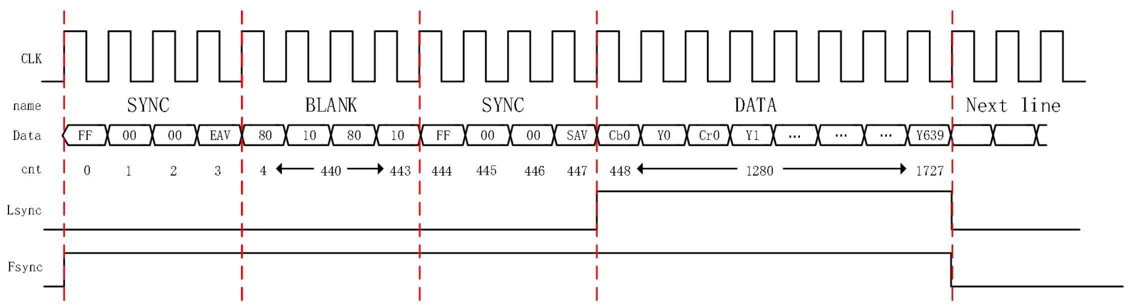


Figure4.6 BT656 Progressive Mode Timing

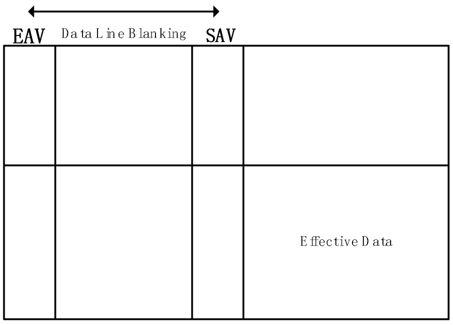


Figure 6 Frame Timing Relationship in Progressive Mode

Table 4.8 BT656 Data Distribution per Frame in Progressive Mode

	0	1	2	3	4-443	444	445	446	447	448-1727
Line	EAV				Invalid	SAV				Valid
0-112	FF	00	00	B6	Y: 10 Cb/Cr: 80	FF	00	00	AB	Y: 10 Cb/Cr: 80
113-624	FF	00	00	9D		FF	00	00	80	YCbCr

BT656 image has 640x512 pixels.

4.6 DVP

Digital Video Port (DVP) is a common digital video interface that allows parallel output. The DVP interface contains 1 clock signal line, 1 frame synchronization (field synchronization) signal line, 1 line synchronization signal line, and 8 parallel data signal lines. When a data frame arrives, the frame synchronization signal goes high, indicating that the next data is the same data frame. When the frame is finished, the frame synchronization signal goes low, indicating the end of the data frame. Similarly, when a line of data arrives, the line synchronization signal goes high, and when the line of data is finished, the line synchronization signal goes low.

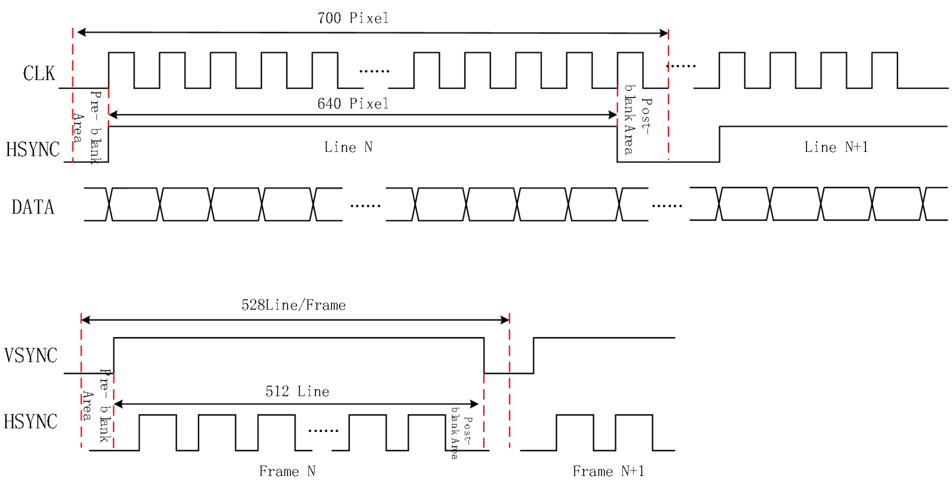


Figure 4.8 DVP Timing Diagram

Table 4.9 DVP Timing Description

No.	Signal	Description	Remarks
1	CLK	Clock	18.75MHz (=700×528×50Hz)
2	DATA	Data	Valid data: 640 pixels×512 lines
3	HSYNC	Line synchronization	There are 700 pixels in one line, of which 640 are valid data, and the remaining 60 are blanking data, with 30 pixels in the pre-blanking area and 30 pixels in the post-blanking area.
4	VSYNC	Frame synchronization	There are 528 lines in one frame, 512 of which are valid data lines, and the remaining 16 are blanking data lines.

4.7 Description of Image Algorithm Processing Delay

Allows digital video output with or without zoom. Delays are shown in Figure 9.

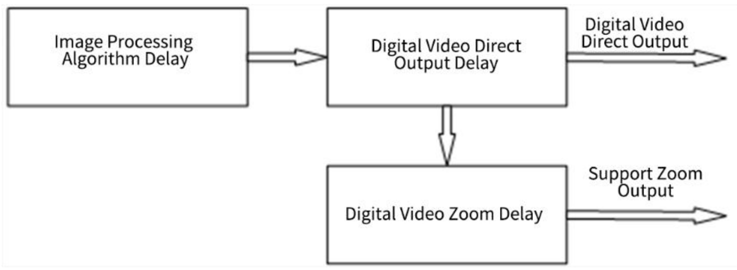


Figure 4.9 Schematic Diagram of Digital Video Output

1. Image processing algorithm delay:

   The processing delay of the NUC module is 1,407 clock cycles, including 700 cycles for each line (two lines) and additional seven cycles.

   The processing delay of the DNS module is 16,825 clock cycles, including 700 cycles for each line (24 lines) and additional 25 cycles.

   The processing delay of the DRC module is 4220 clock cycles, including 700 cycles for each line (6 lines) and additional 20 cycles.

   The clock frequency is 18.75M, and the image processing delay is 1.20ms.
2. Digital video direct output delay: =0ms
3. Digital video zoom delay: ≤40ms (two frames)

   The digital video direct output delay is no greater than 1.20ms, and the digital video zoom delay is no greater than 41.2ms.

5 Structures and Dimensions

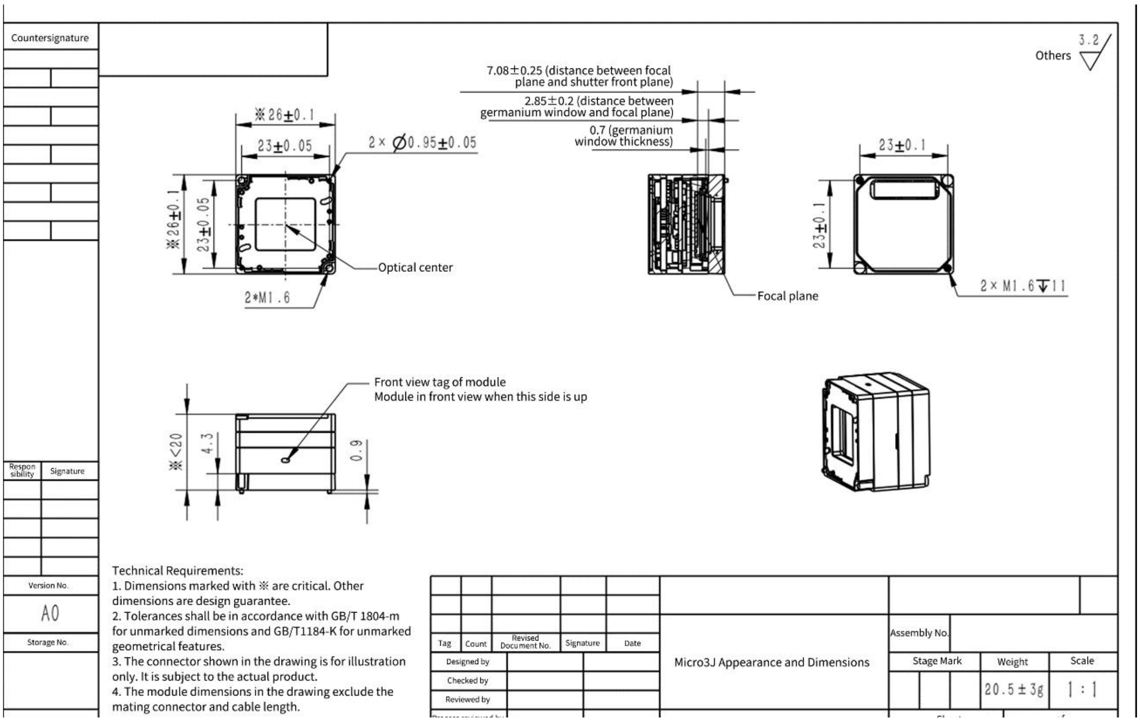


Figure 5.1 Module Dimension

6. Precautions

To protect you and others from injury or to protect your equipment from damage, please read all the following information before using your equipment.

(1) The product shall not face towards the sun or other high-intensity radiation sources directly;

(2) The optimal environment temperature for operating is - 20 ℃ to 50 ℃;

(3) The detector window shall not be touched or hit with hands or other objects;

(4) The equipment and cables shall not be touched with wet hands;

(5) Please do not bend or damage cables;

(6) Scrubbing your equipment with diluents is prohibited;

(7) Do not unplug and plug cables when the power is on;

(8) Wrong cable should not be connected in case that brings damages to the equipment;

(9) Please pay attention to prevent static electricity;

(10) Please do not disassemble the equipment. If there is any fault, please contact us, and professional personnel will carry out maintenance.